REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-4 and 6-15 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the amendments and remarks as set forth below.

Entry of Amendment

Applicants are submitting this Amendment along with a Request for Continued Examination. Accordingly, Applicants submit that the entry of this Amendment is proper and is respectfully requested.

Rejection Under 35 USC 103

Claims 1-4 and 6-15 are rejected under 35 USC 103(a) as being unpatentable over McGuinness (US006104416A) in view of Vinekar (US005581310A). This rejection is respectfully traversed.

The Examiner points out that "With regard to claim 1, McGuinness describes a method of storing an array of digital data into a memory (Col. 3, lines 14-16) having a plurality of memory pages (Col. 8, lines 51-58), the method comprising the steps of dividing the array of digital data into a plurality of block units (Col.3 lines 16-18) each of the block units having a plurality of odd rows and a plurality of even rows (Col. 11, line 51 – Col. 12, line 13), each of the odd rows and the even rows having at least one byte(one byte of storage

is required for each pixel, Col.4, lines 47-48; putting 16 pixels into each row, Col. 11, lines 52-54); storing subsequent odd rows of at least one of the block units into consecutive storage locations in the first memory section (532) (Col. 11, lines 57-63), and storing subsequent even rows of at least one of the block units into consecutive storage locations in the second memory section (534)(Col. 11, line 65-Col. 12, line 13).

However, McGuinness does not specifically teach that each memory page has the first memory section and the second memory section. However, Vinekar describes that each bank contains an odd buffer page section and an even buffer page section (Col. 12, line 46-Col. 13, line11; Figure 8 and 9)." These sections are labeled "odd buffer page 0" and "even buffer page 0", which means that these odd and even sections are on the same page 0, so Bank 0 (800) is considered to contain one page, page 0. Therefore, Vinekar discloses that each memory page (page 0, 800) has a first memory section (odd buffer page 0) and a second memory section (even buffer page 0)."

Memory cells in a typical DRAM memory are physically arranged in a two-dimensional array so that an individual cell can be identified using a combination of a row address and a column address. In other word, each memory cell in the two-dimensional array is addressed by a unique combination of a row address and a column address. To one of ordinary skill in the art, the memory cells within the same row are often collectively referred to as a "page". This definition is found in paragraph [004], lines 29-31 in Published U.S. Application 2004/0155883, "The DRAM can be addressed by the column address and the row address, and **a different row address is addressed to a different page**". And it can be found in Col. 42, lines

53-54 in USP 5384745 filed on Apr. 14, 1993, "**an entire page (one row)**", and in Col. 3, line 6 in USP 5777942 filed on Nov. 8, 1993, "**page (data of a designated one row)**". Also it can be found in col. 3, lines 45-47 in USP 5926839 filed on Nov. 26, 1996, "**a page (here designating a row in the DRAM)**".

While a system accesses data in the memory array, the system activates a "page" (all memory cells in a row) by assigning a row address to the memory. Then, the system assesses the data in the memory cells of the page by assigning at least one column address to the designated memory cell. **Hence, because the Vinekar patent does not illustrate or re-define that the odd buffer page and the even buffer page are parts in a single page, according to the definition used in the art of "page" in memory, the odd buffer page and the even buffer page in Vinekar's patent are different pages and cannot be considered as the first memory section and the second memory section in the present invention**. Instead, the present invention clearly defines that a different row address is addressed to a different page.

According to the Examiner's interpretation of Vinekar's patent, "the odd buffer page section and the even buffer section are on the same page 0", will induce error in the video data processing due to incorrect data in memory cells. Therefore, the odd buffer page 0 and the even buffer page 0 cannot be interpreted to be on the same page 0. And Vinekar does not disclose or teach that the page has a first memory section and a second section.

This reason is illustrated by the following description. As described above, each memory cell in the same page of the memory array is addressed by a unique combination of a row address and a column address. In other words, each memory cell on the same page is

addressed by a unique combination of the row address (designated the page) and a column address which is different from other memory cells'.

In Fig.8 and col. 12, line 46-Col. 13, line 11 in Vinekar's patent, "the **four odd lines** ..... i.e., lines [M1 W0 00, M1 W0 01, M1 W0 02, M1 W0 03], **are written into location 0 (Loc. 0)**, shown in FIG. 8, **across memory segments A, B, C and D, in an odd buffer page (Odd Buffer Page 0, Bank 0)**", "**Similarly, pixel data for even lines** (E0, E1, E2, E3) for these image sub-blocks W0, X0, Y0 and Z0 in half 720 of this same image macroblock **are written**, also with appropriate positional offsets, **into consecutive locations in an even buffer page (Even Buffer Page 0, Bank 0)**. In a similar fashion, **the odd and even lines of pixel data** for half 730 of macroblock M2 (also denoted as 710.sub.2) **are written**, with appropriate positional offsets, **into corresponding locations 4-7 of the odd and even buffer pages, and across memory segments A, B, C and D in bank 0.** Also, in col. 10, lines 14-17, "As all four memory segments, here denoted as **segments A, B, C and D, can be independently addressed for memory locations** that are controlled by two least significant bits of the address bus"

According to the teaching of Vinekar's patent, the odd and even lines of pixel data are written into corresponding odd and even buffer pages, and across memory segments A, B, C and D in Bank 0, wherein memory segments A, B, C and D are independently addressed for memory locations. Therefore, in combination with Examiner's interpretation, the odd buffer page 0 and even buffer page 0 are on the same page 0, i.e. **the odd buffer page 0 and even buffer page 0 can be addressed by the same row address**. And both of the pixel data on odd and even lines are written into corresponding odd even buffer page 0 and even buffer

page 0 and across the same addressable segments A, B, C, and D, i.e. **the pixel data on odd and even lines are written into the same segments with the same column address.**

In consequence, the pixel data on odd and even lines are written into the same memory cells, due to the same row and column address. Therefore, while writing those pixel data into memory, for example, the odd lines of data 00, 01, 02, and 03 are written into the memory first (row address "0" and column address "A, B, C, D"), then the even lines data E0, E1, E2, and E3 are written into the same location (row address "0" and column address "A, B, C, D"). That will cause the original odd lines data to vanish and be substituted by the even lines of data. And it will induce error in the video data processing causing incorrect data. That is why Vinekar disclosed that the odd buffer page and the even buffer page are different pages, shown in col. 12, lines 46-49, "As depicted in tables 800 and 900 in FIGS. 8 and 9, respectively, **the odd and even field portions of both halves of the image macroblocks are written into different odd and even buffer pages**".

Therefore, the odd buffer page 0 and the even buffer page 0 should be interpreted to be different pages, i.e. the different pages corresponding to different row address. It can not be interpreted to be the same page 0. To be precise, the odd buffer page 0 means the "0^{th}" odd buffer page, the even buffer page 0 means the "0^{th}" even buffer page. They are two different pages corresponding to different row address. Hence, Vinekar do not disclose or teach that the page has the first memory section and the second section.

Besides, the Examiner also points out that "However, McGuinness does not specifically teach that each memory page has the first memory section and the second

memory section". That is: each memory page having a first memory section and a second memory section and storing subsequent odd rows of at least one of the block units into consecutive storage locations in the first memory section, and storing subsequent even rows of at least one of the block units into consecutive storage locations in the second memory section. Due to this technical feature, the subject invention can outperform the prior art field-organized storage method such as shown in McGuinness's patent. As described on page 12, lines 13-20 of the present invention, "Compared with the conventional field-organized storage method, since the top field and bottom field of each macroblock are stored in the same page in this embodiment, the number of cross-pages can be substantially reduced since there will be no cross-page penalties when it is required to read both the top and bottom field of the same macroblock. Furthermore, since the top field or bottom field of a macroblock are consecutive addressed in this embodiment, we can easily use DRAM burst access mode to burst access these top field or bottom field and conceal the next row-activation command overhead cycles during current DRAM burst access. Therefore, the effective DRAM bandwidth can be increased."

Furthermore, the present invention includes the features of: "each memory page having a first memory section and a second memory section" and "storing subsequent odd rows of at least one of the block units into consecutive storage locations in the first memory section, and storing subsequent even rows of at least one of the block units into consecutive storage locations in the second memory section". However, both McGuinness's and Vinekar

do not teach or illustrate these features. That is, McGuinness's and Vinekar do not teach or illustrate that each memory page has a first memory section and a second memory section.

In view of the above, Applicants submit that independent claims 1, 10 and 13 are allowable since they are not obvious over the combination of McGuinness and Vinekar. Likewise, claims 2-4, 6-9, 11, 12, 14 and 15 are also allowable based on their dependency from allowable independent claims. In view of this, Applicants submit that all of the claims are now allowable.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejections and allowance of all of the claims are respectfully requested.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: August 18, 2006

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